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EXAMINER	
PORTKA, GARY J	
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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JONATHAN W. HAINES and STEVEN S. WILLIAMS

Appeal 2007-3222
Application 09/894,821
Technology Center 2100

Decided: February 21, 2008

Before LANCE LEONARD BARRY, HOWARD B. BLANKENSHIP, and JAY P. LUCAS, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

This is an appeal arising from the Examiner's final rejection of claims 1, 2, 9, 10, and 20. The Examiner indicates in the Answer that the rejection of claims 1, 2, 10, and 20 has been withdrawn, that claims 1-8 and 20 are allowed, and that claims 10-19 are objected to as being dependent on a rejected base claim. The Examiner sets forth a new ground of rejection

against claim 9 in the Answer. Appellants respond with a reply brief (filed Jul. 19, 2006; "Reply Br.") and thus maintain the appeal, following the requirements of 37 C.F.R. § 41.39(b)(2). We have jurisdiction under 35 U.S.C. §§ 6(b), 134(a).

We affirm.

Appellants' invention relates to the management of buffer memory in a disc drive. (Spec. 1: 10-12.) A traversal engine traverses a linked list in the buffer to determine where to access data in the buffer. (Spec. 2: 15-21.) In traversing the buffer, the traversal engine has traditionally functioned such that each access of a subsequent buffer or cache address was treated as a completely new and independent access to the cache. Thus, even in situations where the engine was to traverse three sequential buffer memory addresses, the engine would release ownership of the buffer and re-arbitrate for access to each subsequent (or next) buffer address location (Spec. 3: 4-10.) In Appellants' method, traversal is configured to take advantage of sequential memory mapping in the buffer (Spec. 8: 3-7), regardless of whether the buffer is managed in a sequential fashion or contains, incidentally, sequential mapping (*id.* at 9: 6-9).

Claim 9 is the sole claim on appeal.

9. A method of managing a data buffer, the method comprising:

(a) receiving a traversal request to traverse the data buffer;

(b) arbitrating for ownership of the data buffer; and

(c) traversing all sequential entries in the data buffer, beginning at an entry point in the data buffer, corresponding to the traversal request prior to voluntarily relinquishing ownership of the data buffer.

The Examiner relies on the following references as evidence of unpatentability:

Krantz	US 6,530,000 B1	Mar. 4, 2003
Berning	US 6,038,619	Mar. 14, 2000
Goodwin	US 5,659,713	Aug. 19, 1997

The Examiner finds that Krantz substantially shows the method set forth by instant claim 9. Krantz, however, does not show that *sequential* entries are traversed. The Examiner turns to Berning, which teaches that data streaming can continue unabated with respect to direct access storage devices (DASDs) when consecutive read or write requests bear a sequential logical address relationship. The sequential relationships avoid interruption of the throughput by the data path being disabled and then enabled with each successive read or write command. Berning, e.g., col. 3, ll. 8-40.

Appellants allege at page 6 of the Reply Brief that Krantz does not teach the combination of claim 9 that includes traversing all sequential entries in the data buffer, with Krantz making no correlation between the unit's access duration and traversal of all sequential entries in the data buffer, neither of which is an issue in controversy. To the extent that Appellants further argue (Reply Br. 6) that Krantz does not teach or suggest arbitration in connection with individual entries in the data buffer, we need only observe that claim 9 requires "arbitrating for ownership of the data

buffer" but is silent with respect to arbitration in connection with individual entries in the data buffer.

Appellants also argue that "[o]ne skilled in the art" understands that using LBAs (logical block addresses) as described by Berning is an addressing scheme used to access the disk 11. Because Berning is deemed to discuss sequential logical addresses in association with cylinders, tracks, and heads in a physical disk, Berning deals with consecutive requests to the disk 11 rather than to data buffer 7, according to Appellants. (Reply Br. 2-3.)

Berning, however, expressly teaches that any *mapping or address translation* between an LBA and the real direct access storage device location (cylinder, track, and head) is performed within the device. Berning col. 2, ll. 59-61. The logical addresses are thus just that -- logical addresses as opposed to physical locations within a DASD. Moreover, as the Examiner points out in the Answer, Berning expressly teaches that the sequential addressing is with respect to the data buffer. Berning col. 5, ll. 30-43. We do not find any attempt at a response in the Reply Brief to Berning's teachings at column 5. Appellants' position thus rests on mere allegation, which does not demonstrate error in the Examiner's rejection.

The Examiner offers Goodwin as evidentiary support that streaming data requires sequential access. (Ans. 3-4.) We consider the teachings of Goodwin to be merely cumulative because Krantz and Berning are sufficient

to demonstrate prima facie unpatentability of the invention as broadly claimed.

Berning expressly teaches the use of sequential address relationships in a data buffer to avoid interruption of the throughput by the data path being disabled and then enabled with each successive read or write command. Appellants' suggestion (Reply Br. 6) that the references do not teach or suggest "how" Krantz would be modified in accordance with the teachings of Berning might be regarded as the embryonic stage of a response to the rejection for prima facie obviousness of the subject matter of instant claim 9. However, Appellants do not offer any evidence, or even any reasoning, as to why one skilled in the art would be at a loss to combine the teachings of the two references, or that the combination would be "uniquely challenging or difficult for one of ordinary skill in the art." *See Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1740-41 (2007)). In any event, it is not necessary that the inventions of the references be physically combinable to render obvious the invention under review. *In re Sneed*, 710 F.2d 1544, 1550 (Fed. Cir. 1983).

Moreover, Appellants' disclosure (Spec. 2: 14 - 3: 12) indicates that the problem in the prior art was the requirement of releasing ownership of the buffer and re-arbitrating for each subsequent buffer address location -- the problem that is solved by Berning.

We are thus not persuaded that claim 9 has been rejected in error. We sustain the rejection.

CONCLUSION

The rejection of claim 9 under 35 U.S.C. § 103(a) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. §1.136(a).

AFFIRMED

pgc

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